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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,008	07/03/2002	Gilbert Wolrich	10559-311US1	5753

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,008	WOLRICH ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-8,10-14 and 17-26* is/are pending in the application.

4a) Of the above claim(s) *5,9,15 and 16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6-8,10-14 and 17-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/13/04, 12/06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Clams 1-4,6-8, 10-14,17-26 are presented for examoinatiopn. Claims 5, 9,15,16 have been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4,5,6-9,11-14, 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama (5,928,358) in view of Hasegawa (5,724,563) .

3. As to cliams 1,9, 20, 22, taught at leasy :

a) executing a branch instruction [20] in executon of an instruction stream (see the sequence of progrma in col.7, lines 32-37) with a branch based on a bit (I bit branch prediction 20b) specified in the branch instruction of a register specified in the branch instrulction being set or cleared (see col.7, lines 38-51) , and including a first token [20d] that specified destination addres of instruction in the instruction stream that are after the branch instruction to execute and a second token that specified a branch guess operation (see the frequency of tken branch in the history in col.7, ines 52-63 as the guess informaiton, for xecution see instruciton execution in col.8, lines 49-65).

b) decode logic (see col.13, lines 1-13).

4. Takayama did not specifcally teach this first token was used for specifying number of of instruction in the instruction stream that are after the branch instruction to execute before performing the branch operation as claimed. However, Hasegawa taught a first token was used for specifying number of of instruction (3) in the instruction stream that are after the branch instruction to execute before performing the branch operation (see fig.10, number 3 specified in the branch instruciton , see S1-S3 instructions, see the 3 instrucitons after the branch and executed before branch execution to X in col.12, lines 32-46, see different number in col.6, lines 25-33). It would have been obvious to one of oridary skill in the art to use Hasegawa in Takayama for icludinghte fisrt token for specifying number of of instruction in the instruction stream that are after the branch instruction to execute before performing the branch operation as claimed because the use of Hasegawa could provide Takayama the ability to determine the number of instrucitns to be executed after the branch before performing the branch ,. Thereby , predict the latency before the branch operaitn, and it could be achieved by predefininghte n first token of Hasegawa into the configuration file of Takayama with modified cntrol parameters (e.g. the token length, type etc.) so that the first token of Hasegawa specifyuinghte num,ber of instrcuitns after the branch instrucion could be recognized by Takayama, and becuiase Takayama also taught fetching and predread of a next insttrcution asfter the branch during the seocn half of the clock cycle before performing the branch (see col.13, lines 20-28), which was a suggstonof the need for detrei nint

number of instrucons cycles, and therfore the number of instrucins before executingh ebran operation, in doing so, provided a motivation.

5. As to claims 2,23, see the frequency of tken branch in the history in col.7, ines 52-63 as the guess informaiton, for xecution see instruciton execution in col.8, lines 49-65.

6. As to cliams 3, 4, Hasegawa also included a defer-I causing execution of ith instruciton (see the branch after x instructions specified in the branch instruction format in fig.2, see the field for storing the number of instructions, see also fig.5, and fig.10B, and fig.5B the numerical value 3, the ith, or the counter value counting down the order of instructions , see also the number 3 and 4 in the branch instruction in fig.10B) .

7. As to claim 5, see fig.1 and fig.3 of Takayama. As to the optional token specifying the number of instrucitns to execute before the branch performing the branch , see discussons to claim 1 above.

8. As to claims 6,7, Takayam taught his ivention was realiaed not only by hardware, but also software (see col.5, lines 5-6). Therefore, tokens by progrmmer or assembler program was also applicable in Takayama.

9. As to claims 8, Hasegawa also included unconditional branch (see col.5, lines
50-53) and ALU conditional branch (see the arithmetic flags in col.1 1, lines 19-52).

10. As to claim 11, Takayam also inlcuded a specified context (see the branch histry informatiuon in fig.3, see fig.4 for details). Hasegawa also included a specified context (see the number of instructions 3 in the Branch after 3 X in fig.5).

11. As to claim 12, Takayam also icluded a selected value (see the predicted bit). In additin, Hasegawa also included a selected state name of a selected value (see the opcode value in Table 1 col.1 1).

12. As to claim 13, see Takayam's predicted bit . See also Hasegawa's deasserted specified signal (see the "0" or "1" in the flag in col.1 1 , lines 32).

13. As to claim 14, Takayam also included a guess-branch token (see branch history field in fig.3).

14. As to claim 17, Takayama taught executing a branch instruction that causes a branch operation in an instruction stream based on any specified value being truç or false (see the execution unit judgi the condition of the branch instrcuin in col.13, ines 29-39).

15. As to the deferring of the branch performance based' on the token specifying number of instructions , Takayam did not specficaly disclose the deferring of a branch based on specied nubemr as clamed. However, Hasegawa also included deferring the branch operation based on the token number specified in instruction (see the branch instruction format in 2, see the field for storing the number of instructions, see also fig.5, and fig.10B, and fig.5B the numerical value 3, or the counter value counting down the order of instructions ,

see also the number 3 and 4 in the branch instruction in fig.10B) . The reaossn of obviusmness ahcve been given in paragraph above, thereo iot wil not be repeated herein.

16. As to claim 18, Takayam also branch tken rather than the next instrucion (se the taken branch in col.14, ines 49-67).

17. As to claim 19, see paragpraph above. See also Hasegawa's compiler top fill the delay cycles (see col.3, lines 20-24).

18. As to claim 20, see the count value for defiing the timing of predictive branch instrucion in col.7, ines 8-19 in Hasegawa.

19. As to claim 21, Hasegawa was also directed to efficiency of program coding (see the application program in col.1, lines 42-48 , col.3, lines 25-32 for background).

20. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takayama (5,928,358) in view of Hasegawa (5,724,563) and as applied to claim 1 above, and further in view of Khim Yeoh et al. (5,274,770).

21. As to claim 10, limitation of the parent claim 1 have been discussed in previous paragraph , therefore, it will not be repeated herein. Neither Takayam nor Hasegawa specifically showed the match or mismatch of the byte compare value as claimed. However, Khim Yeoh disclosed a system for performing a conditional branch based a comparison of values in bytes (see col.3, lines 15-

18). It would have been obvious to one of ordinary skill in the art to use Khim Yeoh in Takayam for including the match and mismatch (i.e. comparison) of the byte compare value as claimed because the use of Khim Yeoh could expand the processing structure of Takayam to accept additional conditional parameters, such as the conditional code of more than 4 bits, thereby enhancing the adaptability of the system bus, and because Takayam also tauhgt the hardware size could be reduced to realize his branch porediction (see col.2, lines 61-67), which was recognizable by one of ordinary skill in the art that determination or comparison of hardware size, such as word, byte, bit should be also applicable in Takayam , and for the above reasons provided a motivation.

22. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takayama (5,928,358) in view of Hasegawa (5,724,563) and as applied to claims 1, 17, 22 above, and further in view of Chrysos (5,923,872)

23. As to claims 24-26, neither Takayam nor Hasegawa specifically teach the hardware based multi threaded as claimed. However, Chrysos disclosed a system including hardware contexts for simultaneously multithreaded execution (see col.12, lines 15-18).

24. It would have been obvious to one of ordinary skill in the art to use Chrysos in Takayama for including the hardware based multi threaded as claimed because the use of Chrysos could provide Takayama the capability to adjust to specific hardware construct of the branch prediction, and it could be readily achieved by configuring the hardware parameters of Chrysos (or the

contexts) into Takayama so that the specific hardware based multithreads of Chysos could recognized by Takayama, and because Takayama was also directed to the pipelined branch instructions (see col.7, lines 18-22), which was a suggestion of the need for including multiple executable threads in order to achieve the efficiency of the pipelined process in Takayama, in doing so, provided a motivation. As to the hardware base , see the bit level of the condition codes in fig.9.

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Brodnax et al. (5,463,746) is cited for a guess branch token (see fig.4 [GUESS], see also col.4 , lines 26-43 for the guess bit embedded into the branch instruction).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new

number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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